

Hall Ticket Number:

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Code No. : 13268 N/O

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD*Accredited by NAAC with A++ Grade***B.E. (CSE & AIML) III-Semester Main & Backlog Examinations, Jan./Feb.-2024****Computer Architecture**

Time: 3 hours

Max. Marks: 60

*Note: Answer all questions from Part-A and any FIVE from Part-B**Part-A (10 × 2 = 20 Marks)*

Q. No.	Stem of the question	M	L	CO	PO
1.	The 8 bit register AR, BR, CR and DR initially have the following values: AR=11110000 BR=11111111 CR=10111001 DR=11101010 Determine the 8-bit values in each register after the execution of the following sequence of micro operations: AR ← AR+BR CR ← CR AND DR	2	2	1	1,2
2.	Draw a diagram of a bus system similar to three state buffers and a decoder instead of the multiplexer?	2	2	1	1,2
3.	Describe the difference between a direct and an indirect address instruction and discuss how many references to memory are needed for each such type of instruction to bring an operand into a processor register?	2	2	2	1,2
4.	Draw a timing diagram assuming that SC is cleared to 0 at time T ₃ if control signal C ₇ is active. $C_7T_3: SC \leftarrow 0$	2	3	2	1,2
5.	Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the result. $(5 * 4) [8 (12 - 4) + 2]$	2	2	3	1,2
6.	Distinguish External interrupts and Internal interrupts and give an example for each.	2	2	3	1,2
7.	Define about Cycle Stealing and Burst mode transfers in DMA controller.	2	1	4	1,2
8.	Indicate whether the following constitute a control, status, or data transfer commands. a. Skip next instruction if flag is set. b. Seek a given record on a magnetic disk. c. Check if I/O device is ready. d. Move printer paper to beginning of next page.	2	3	4	1,2
9.	Explain about locality of reference and also discuss about hit ratio associated with cache memory.	2	1	5	1,2

Contd... 2

10.	<p>A computer uses RAM chips of 1024 x 1 capacity</p> <p>a. how many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?</p> <p>b. How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.</p>	2 2 5 1,2
<p>Part-B (5 × 8 = 40 Marks)</p>		
11. a)	<p>The outputs of four registers, R0, R1, R2, and R3, are connected through 4-to-1-line multiplexers to the inputs of a fifth register, R5. Each register is eight bits long. The required transfers are dictated by four timing variables T0 through T3 as follows:</p> <p>T0: R5 ← R0 T1: R5 ← R1 T2: R5 ← R2 T3: R5 ← R3</p> <p>The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of register R5.</p>	4 3 1 1,2
b)	<p>Explain in detail the application of the micro-operations to perform the following with suitable example and also mention the logic operation used in each case.</p> <p>i) Selective set ii) Selective Clear iii) Selective complement iv) Mask</p>	4 2 1 1,2
12. a)	<p>A computer uses a memory unit with 1024K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.</p> <p>i. How many bits are there in the operation code, the register code part, and the address part respectively?</p> <p>ii. Draw the instruction word format and indicate the number of bits in each part.</p>	4 3 2 1,2
b)	<p>Explain the following memory-reference instructions and write the micro-operations along with the control and timing signal needed to perform each of these instructions:</p> <p>i) ADD ii) STA iii) BUN iv) AND</p>	4 2 2 1,2
13. a)	<p>Evaluate the following expression using one-address, two-address and three-address instruction formats and mention the advantage of using three-address format.</p> <p>(P+Q)*(R+S)</p>	4 3 3 1,2

b)	Differentiate RISC and CISC architectures and describe their main characteristics in detail.	4	1	3	1,2									
14. a)	Discuss the disadvantage of using Strobe pulse method of asynchronous transfer mode and how we can overcome that by using Handshaking method. Also explain the data transfer procedure when initiated by the source with a neat diagram.	4	2	4	1,2									
b)	Explain Priority interrupt and discuss about Polling and Daisy-chaining Priority mechanisms. Also Illustrate Daisy chaining mechanism by connecting three devices with CPU with a neat diagram.	4	2	4	1,2									
15. a)	A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1K words. The following page reference changes occur during a given time interval. (Only page changes are listed. If the same page is referenced again, it is not listed twice.) 4 2 0 1 2 6 1 4 0 1 0 2 3 5 7 Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (a) FIFO; (b) LRU.	4	3	5	1,2									
b)	Discuss the differences between main memory and auxiliary memory and also explain about magnetic disks and magnetic tapes in detail.	4	2	5	1,2									
16. a)	Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in} . Draw the logic diagram for the first two stages.	4	3	1	1,2									
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>S</th> <th>$C_{in}=0$</th> <th>$C_{in}=1$</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>$D=A+B$(add)</td> <td>$D=A+1$ (increment)</td> </tr> <tr> <td>1</td> <td>$D=A-1$ (decrement)</td> <td>$D=A+B+1$ (subtract)</td> </tr> </tbody> </table>	S	$C_{in}=0$	$C_{in}=1$	0	$D=A+B$ (add)	$D=A+1$ (increment)	1	$D=A-1$ (decrement)	$D=A+B+1$ (subtract)				
S	$C_{in}=0$	$C_{in}=1$												
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1	$D=A-1$ (decrement)	$D=A+B+1$ (subtract)												
b)	Define control word & control memory and explain the general configuration of a microprogrammed control unit in detail with a neat diagram.	4	1	2	1,2									
17.	Answer any <i>two</i> of the following:													
a)	Explain in detail how addition and subtraction of signed magnitude numbers are performed in computer arithmetic using flow chart.	4	2	3	1,2									
b)	Differentiate Programmed I/O and Interrupt-initiated I/O and discuss about them in detail.	4	2	4	1,2									
c)	Explain the following mapping procedures for organizing cache memory: a) Associative mapping b) Direct mapping c) Set-associative mapping	4	1	5	1,2									

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%
